What is claimed:

1. A solid-state imaging device comprising:

a photosensor for collecting charge created by incident photons; and

a comparator for comparing a digital voltage value corresponding to the collected charge, to a predetermined value, and generating a compare output.

2. The solid-state imaging device of Claim 1 further including a normalizing circuit for normalizing the digital voltage value, in response to the comparison output, and outputting a normalized voltage value.

3. The solid-state imaging device of Claim 1 wherein the photosensor is an array of photodetectors.

4. The solid-state imaging device of Claim 3 wherein the photodetectors are CMOS devices.

5. The solid-state imaging device of Claim 3 further including at least one digital voltage value corresponding to the charge stored in each photodetector.

6. The solid-state imaging device of Claim 5 further including a frame memory for storing the normalized voltage values.

7. The solid-state imaging device of Claim 6 further including a timing control unit for controlling sequencing of the photodetectors.

8. The solid-state imaging device of Claim 7 wherein the timing control unit includes an array sequencer and an exposure logic unit.

9. The solid-state imaging device of Claim 8 further including an indexer for providing an index number to the normalizing circuit.

10. The solid-state imaging device of Claim 9 further comprising a data bus for transferring data between the frame memory and the comparator.

11. The solid-state imaging device of Claim 10 wherein the normalizing circuit is a programmable shifter.

12. The solid-state imaging device of Claim 11 wherein the programmable shifter shifts the digital voltage values by a predetermined number of bits.

13. The solid-state imaging device of Claim 12 wherein the predetermined number of bits is equal to the index number.

14. The solid-state imaging device of Claim 13 wherein the normalizing unit is a barrel shifter.

15. The solid-state imaging device of Claim 7 wherein the timing control unit comprises a first output corresponding to a row-number of the array of photodetectors, and a second output corresponding to a column-number of the array of photodetectors.

16. A method of generating digital images having improved dynamic range comprising:

collecting a charge in a photodetector by exposing the photodetector with photons for a first predetermined period of time;

comparing the charge to a predetermined value;

if the charge is greater than or equal to the predetermined value, storing a digital voltage value corresponding to the charge; and

if the charge is less than the predetermined value, collecting additional charge in the photodetector by re-exposing the photodetector for a new period of time.

17. The method of claim 16 further including non-destructively reading the charge.

18. The method of claim 17 further including normalizing the digital voltage value to generate a normalized voltage value.

19. The method of claim 18 wherein the step of storing comprises storing the normalized digital value.

20. The method of claim 19 wherein the step of storing further comprises storing the normalized voltage value in a location in a frame memory.

21. The method of claim 20 further including clearing the location in the frame memory before collecting the charge.

22. The method of claim 21 wherein the step of storing the normalized voltage value in the location in the frame memory comprises storing the normalized voltage value in the location in the frame memory only if the location in the frame memory is blank.

23. The method of claim 22 further including incrementing an index number before collecting additional charge in the photodetector.

24. The method of claim 23 wherein the normalizing step comprises shifting the digital voltage value to the right by a predetermined number of bits.

25. The method of claim 24 wherein the normalizing step comprises shifting the digital voltage value to the right by a number of bits equal to the index number.

26. The method of claim 25 further including storing the normalized voltage value, if the charge is less than the predetermined value, and if the index number is greater than a predetermined index value.

27. The method of claim 25 further including storing the normalized voltage value, if the charge is less than the predetermined value, and if the index number is greater than a width of the location in the frame memory.

28. The method of claim 19 wherein the step of collecting additional charge comprises re-exposing the photodetector with photons for a period of time equal to

$x*2^{(N-1)}$

where x is equal to the first predetermined period of time and N is equal to the index number.

29. A solid-state imaging device comprising:

means for collecting charge created by incident photons; and

means for comparing a digital voltage value corresponding to the collected charge, to a predetermined value, and generating a comparison output.

30. The solid-state imaging device of Claim 29 further including a means for normalizing the digital voltage value, in response to the comparison output, and outputting a normalized voltage value.

31. The solid-state imaging device of Claim 29 wherein the collecting means is an array of photodetectors.

32. The solid-state imaging device of Claim 31 wherein the photodetectors are CMOS devices.

33. A system for generating digital images having improved dynamic range comprising:

means for collecting a charge in a photodetector by exposing the photodetector with photons for a first predetermined period of time;

means for comparing the charge to a predetermined value;

means for storing a digital voltage value corresponding to the charge if the charge is greater than or equal to the predetermined value; and

means for collecting additional charge in the photodetector by re-exposing the photodetector for a new period of time if the charge is less than the predetermined value.

34. The system of claim 33 further including means for non-destructively reading the charge.

35. The method of claim 34 further including means for normalizing the digital voltage value to generate a normalized voltage value.